REMARKS

This Amendment is filed in response to the Office Action dated August 10, 2004. For the following reasons this application should be allowed and the case passed to issue. No new matter is introduced by this amendment. The amendment to claim 13 is supported by originally filed claim 14.

Claims 1-13 and 15-18 are pending in this application. Claims 1-12 have been withdrawn pursuant to a restriction requirement. Claims 13-18 have been rejected. Claim 13 has been amended and claim 14 canceled in this response.

Objection to the Specification

The Examiner objected to the specification for allegedly failing to provide proper antecedent basis in the specification for the recited "said semiconductor layer" in claim 15. This objection is traversed, and reconsideration and withdrawal thereof respectfully requested. There is antecedent basis for said semiconductor layer in the specification as the "semiconductor layer" is recited in the specification at lines 2 and 30 of page 3.

Claim Rejections Under 35 U.S.C. § 102

Claims 13-18 are rejected under 35 U.S.C. § 102(b) as being anticipated by Hayashi (JP 6-318561).

Claims 13-18 are rejected under 35 U.S.C. § 102(e) as being anticipated by Minato et al. (U.S. PG-Pub 2003/0132450).

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 1, is a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer. Each semiconductor element has a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain. The method comprises the steps of

implanting impurities concurrently into at least a predetermined part of the drain of one semiconductor element and into a predetermined part of the drain of another semiconductor element. An implantation mask is used that includes a portion corresponding to the drain of the one semiconductor element and has a first opening ratio as well as a portion corresponding to the drain of the another semiconductor element and has a second opening ratio different from the first opening ratio. The one semiconductor element has a breakdown voltage higher than that of the another semiconductor element. The implantation mask used has the first opening ratio smaller than the second opening ratio. The integrated semiconductor device is annealed after the step of implanting impurities to diffuse the impurities.

The Examiner asserts that Hayashi (Figs. 1-4) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources and drains, and implanting impurities through an implantation mask having different opening ratios (A, A'). The Examiner further asserts that Hayashi discloses that the semiconductor elements have different breakdown voltages, and that the masks illustrated in Fig. 4 include stripe-shaped masks and masks with dot-like openings.

The Examiner avers that Minato (para. [0113] and Figs. 100-116) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources 6 and drains 3, and implanting impurities through an implantation mask 41 having different opening

ratios (para. [0112] and claim 36). The Examiner further avers that Minato discloses that the semiconductor elements have different breakdown voltages, and that the masks include stripe-shaped masks (para. [0396] and [0404]). The Examiner concluded that claims 17 and 18 do not further limit the method.

Hayashi and Minato, however, do not anticipate the claimed invention. Neither Hayashi nor Minato disclose the claimed method of manufacturing an integrated semiconductor device wherein the one semiconductor element has a breakdown voltage higher than that of the another semiconductor element, and that the implantation mask used has a first opening ratio smaller than the second opening ratio, as required by claim 13. Thus, the mask having the smaller opening ratio is used for fabricating the semiconductor element of a higher breakdown voltage.

Hayashi discloses a method of manufacturing an integrated semiconductor device using a mask having different opening ratios (A, A') for implanting impurities in Figs. 1-4. Hayashi merely teaches, as regions for adjusting the concentration of impurities, "MOS transistor formation scheduled regions" or "the concentration of the impurity areas where impurities are to be implanted" and does not teach anything concerning the specific locations of MOS transistors. In addition, Hayashi does not disclose that one semiconductor element has a breakdown voltage higher than that of the another semiconductor element and that the implantation mask used has the first opening ratio smaller than the second opening ratio.

Furthermore, although Minato discloses a semiconductor structure with a guard ring in the same transistor, there is no disclosure regarding the impurity concentration of the drain of the MOS transistor in Minato.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 399, 36 USPQ2d 1101 (Fed. Cir. 1995); *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). Because neither Hayashi nor Minato disclose the one semiconductor element has a breakdown voltage higher than that of the another semiconductor element, and that the implantation mask used having the first opening ratio smaller than the second opening ratio, as required by claim 13, Hayashi and Minato do not anticipate claim 13.

Applicants further submit Hayashi and Minato, whether taken alone, or in combination do not suggest the claimed method of manufacturing an integrated semiconductor device.

The dependent claims further distinguish the claimed invention. For example, claim 15 further requires that the one semiconductor element is adjacent to the another semiconductor element, and the method further comprises the step of providing, in the semiconductor layer, a wall-shaped element-isolation insulating film for isolating the one semiconductor element from the another semiconductor element, prior to the step of implanting impurities. Claim 16 further requires that the implantation mask has masking portions and openings in the shape of stripes, and the implantation mask is used by being placed with the stripes arranged in the direction parallel to a carrier path from the source to the drain of the semiconductor elements. The cited prior art does not suggest the claimed method with these additional limitations.

The Examiner's conclusion that claims 17 and 18 fail to further limit the claimed method is incorrect. Claim 17 further requires that the implantation mask used is a mesh implantation mask having dot-like openings dispersed in a masking portion. Claim 18 further requires that the implantation mask being used is a dot implantation mask having dot-like masking portions dispersed in an opening. Clearly, claims 17 and 18 further limit and distinguish the claimed method.

In light of the above Amendment and Remarks, this application should be allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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